

Stress and Characterization Strategies to Assess Oxide Breakdown in High-Voltage GaN Field-Effect Transistors

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Abstract

GaN metal-insulator-semiconductor high electron mobility transistors (MIS-HEMTs) are promising for high-voltage power switching applications. A concern with this new device technology is oxide reliability under prolonged high-field and high-temperature conditions. This paper studies an important aspect of oxide reliability, time-dependent dielectric breakdown (TDDB) in GaN MIS-HEMTs. We have developed an experimental methodology to characterize TDDB through time-dependent current-voltage and capacitance-voltage measurements. Our techniques isolate and observe different roles of V_T shift, oxide trap formation and trapping, interface state generation, stress-induced leakage current (SILC), and eventual breakdown.

INTRODUCTION

As the demand for more energy efficient electronics increases, GaN Field-Effect Transistors (FETs) have emerged as promising candidates for high-voltage power management applications. Though GaN has excellent material properties, there are still many challenges to overcome before GaN transistors are ready for commercial deployment [1]–[3]. Our work focuses on gate oxide reliability and in particular, in contributing fundamental understanding behind the physics of time-dependent dielectric breakdown (TDDB) of the gate oxide, a catastrophic condition that arises after prolonged high-voltage gate bias stress [4]. Towards this end, we are investigating stress-characterization techniques that allow transistor characterization during stress experiments. We leverage a rich body of work that has been performed on silicon MOSFETs with regards to TDDB [5].

There are several challenges involved in carrying out TDDB studies in GaN metal-insulator-semiconductor high electron mobility transistors (MIS-HEMTs), the prevailing device structure for power applications. First, the gate stack contains multiple layers and several interfaces. This gives rise to a somewhat uncertain electric field distribution. Second, there can be complex dynamics involved as there is potential electron trapping in the AlGaN barrier [6], in the gate oxide and at their interface [7], and electron

accumulation at the AlGaN/oxide interface is known to respond rather slowly [7]. These complex dynamics result in a rather unstable and fast changing threshold voltage, V_T , a significant complication in these types of experiments [7]. Finally, with the current state of maturity of the technology, it is not obvious how to develop a characterization suite that is at the same time comprehensive and benign so that it can be used repeatedly without damaging the device.

This paper describes our research in developing suitable experimental techniques to characterize the physics of TDDB and our early results.

I-V TDDB EXPERIMENTS

The devices studied in this work are industrially prototyped AlGaN/GaN MIS-HEMTs fabricated on a 6-inch wafer. They feature three field plates placed in a stairway fashion along the gate-to-drain gap and they have a breakdown voltage >600 V. All experiments were carried out on an Agilent B1505A Power Device Analyzer equipped with High Power Source Measurement Units (HPSMUs) and a Capacitance Measurement Unit (CMU).

Fig. 1 shows the evolution of the gate current, I_G , in a typical constant-voltage TDDB experiment at $V_{Gstress}=13.5$ V with $V_{DS}=0$ V, as well as the stress-induced leakage current (SILC) extracted using the methodology in [8]. As time increases, I_G increases and eventually oxide breakdown takes

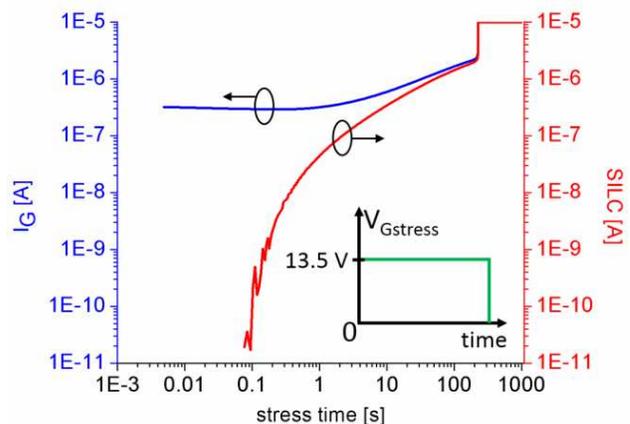


Fig. 1. Gate leakage current (blue) and SILC (red) as a function of stress time during a constant $V_{Gstress}$ TDDB experiment. The FET is held at $V_G=13.5$ V until the device breaks down. $V_{DS}=0$ V.

place at around 225 s. Other than the time to breakdown and the observation of SILC that takes place throughout most of the experiment, there is little insight gained from these measurements.

We enhance this technique by pausing the TDDB stress and periodically characterizing the device by examining the I-V characteristics, as depicted in the inset of Fig. 2. To validate this approach, we exploit a unique feature of TDDB identified in silicon MOSFETs that the charge to breakdown of a MOS gate stack, Q_{BD} , is constant, regardless of stress conditions [5]. By extension, under constant stress voltage the time to breakdown, t_{BD} , should also be a constant. We carry out TDDB experiments to verify this hypothesis following the conventional approach, and also under the new scheme with stress interruptions every 30 s where we measure the subthreshold I-V characteristics at $V_{DS}=0.1$ V in a hysteresis sweep, shown in Fig. 2. The hysteresis sweep is to confirm that V_T does not shift significantly during measurement. The statistical results for t_{BD} in the Weibull plot of Fig. 3 exhibit a classic shape and indicate that the added complexity has not affected the breakdown measurements.

Our new scheme that includes stress interruption and characterization provides new insights. In the subthreshold

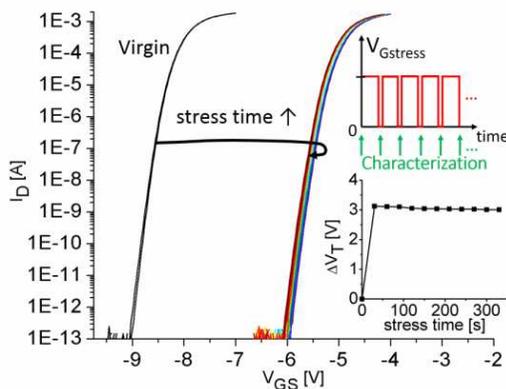


Fig. 2. Subthreshold characteristics at $V_{DS}=0.1$ V, for a TDDB experiment at $V_{Gstress} = 13.5$ V. I-V characterization is performed every 30 s as a hysteresis sweep to confirm V_T does not shift during measurement.

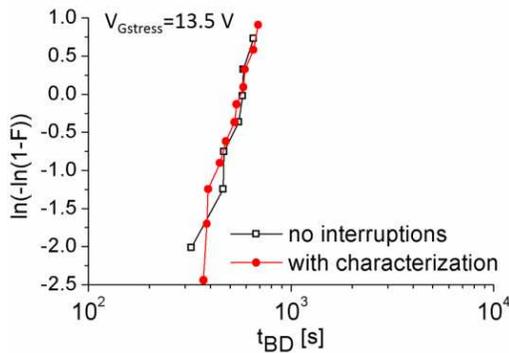


Fig. 3. Weibull plot of device breakdown for experiments with constant $V_{Gstress} = 13.5$ V and no pauses for characterization (black), as well as experiments that utilize pauses during stress to characterize the device (red). F is defined as the fraction of devices that have reached breakdown.

characteristics obtained during a typical experiment (Fig. 2) we observe an initial large positive V_T shift followed by a slower negative V_T shift as the stress continues (see inset). This positive V_T shift has been observed by other authors [7], [9]-[10] and is attributed to oxide trapping. The subthreshold swing shown in Fig. 4 also exhibits an immediate increase from the virgin state right after the stress has been applied, but it then stays roughly constant for the remainder of the stress experiment and shows no real trend during this time. These results suggest interface state generation early in the stress experiment in addition to electron trapping in the oxide or the AlGaN barrier.

Closer probing of the early stages of stress can be gained through a step-stress experiment where $V_{Gstress}$ is stepped up (inset of Fig. 5b). In an experiment of this kind, the evolution of I_G during stress, Fig. 6, reveals that for low values of $V_{Gstress}$, I_G tends to drop with time during a given stress step. This can be attributed to electron trapping in the oxide or the AlGaN barrier. Beyond around $V_{Gstress} \sim 12.5$ V, I_G increases during each stress phase. This is a manifestation of SILC and in our case correlates with the turnaround of the V_T shift which initially is positive but at around $V_{Gstress} = 12.5$ V, begins to turn negative (Fig. 5a). We also see an increase in the subthreshold swing (Fig. 5b) as the step-stress progresses, but its most notable degradation takes place after $V_{Gstress} = 12.5$ V.

From these results, we can postulate that below $V_{Gstress} = 12.5$ V, electron trapping in the oxide or the AlGaN are the dominant effects, while for higher values of $V_{Gstress}$, trap generation at the oxide/semiconductor interface and in the oxide take place and the oxide is eventually driven into breakdown.

C-V TDDB EXPERIMENTS

We have sought to further the information that we extract from TDDB experiments by introducing C-V characterization. We accomplish this by using the Capacitance Measurement Unit (CMU) of our measurement

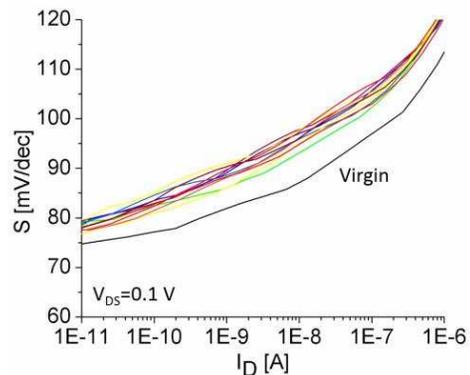


Fig. 4. Subthreshold swing vs. drain current corresponding to I-V characteristics of Fig. 2, from the average of each hysteresis sweep of the transfer characteristics. There is a fixed degradation of S at the beginning of the experiment, which then stays roughly constant with no noticeable trend until breakdown. I-V characterization is performed every 30 s.

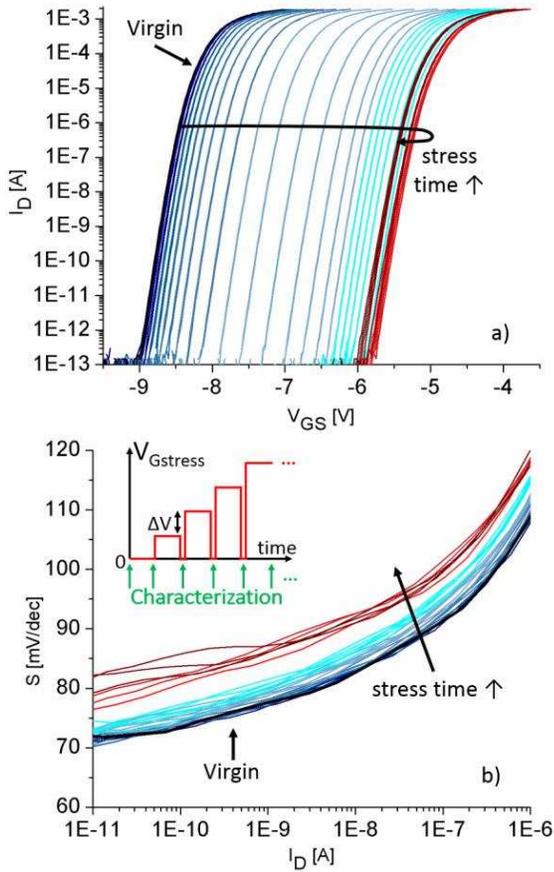


Fig. 5. a) Subthreshold characteristics and b) corresponding subthreshold swing for a TDDDB step-stress experiment. S is acquired from the average of each hysteresis sweep of the transfer characteristics. $V_{Gstress}$ begins at 0 V and increases in 0.5 V increments every 30 s until the device breaks down. $V_{DS}=0.1$ V.

system to both apply stress and to characterize the device. This scheme allows us to monitor the capacitance evolution during the stress portion of the experiment, and also to carry out detailed C-V measurements when the stress has been paused.

The capacitance evolution during the stress phase of multiple constant stress experiments at $V_{Gstress} = 13.5$ V is shown in Fig. 7. At this high value of V_G , the capacitance as well as capacitance frequency dispersion increase as the stress time increases. Both effects are consistent with charge trapping in newly created states in the oxide with the measurement frequency impacting the distance into the oxide that traps can respond to the AC signal [11].

Similar C-V characterization during a step-stress experiment in Fig. 8 portrays a very rich picture. For low $V_{Gstress}$, a rapid drop in C_{GG} takes place during each stress step. This is probably due to oxide or AlGaN trapping but the detailed mechanism is unclear. Regardless, we can trace out the C-V characteristics for $V_G > 0$ V by looking at C_{GG} at the beginning of each stress step. This correlates with measured standard C-V characteristics up to $V_{GS}=13$ V as

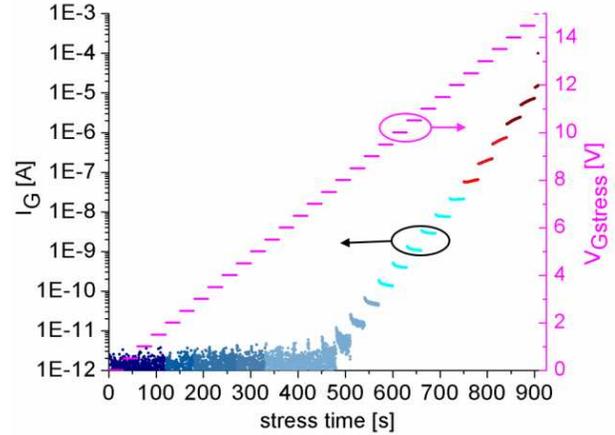


Fig. 6. I_G vs. stress time during a V_G step-stress experiment. $V_{Gstress}$ is shown on the right axis for scale. $V_{DS}=0$ V.

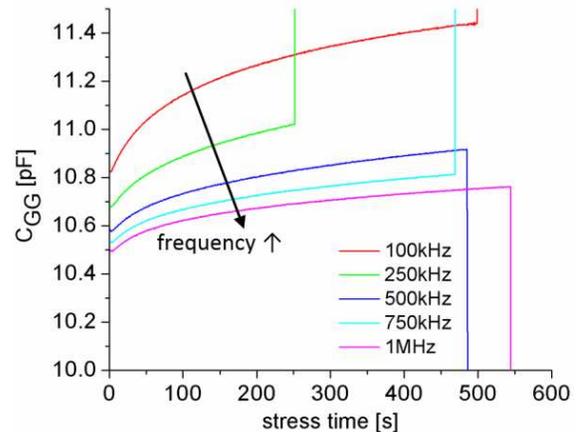


Fig. 7. Gate capacitance evolution over stress time at various frequencies in a constant V_G stress experiment. C_{GG} is measured at $V_{Gstress}=13.5$ V.

shown in the inset of Fig. 8. At higher $V_{Gstress}$, the capacitance increases during stress just as I_G did in the identical step-stress experiment of Fig. 6. This is another manifestation of the effect observed in Fig. 7 and reveals large trap formation in the oxide that precedes device breakdown.

DISCUSSION

Thus far, our experimentation has revealed a rich picture of oxide breakdown in GaN MIS-HEMTs. The statistical behavior is consistent with that seen in Si devices. In a classic TDDDB experiment, we observe the evolution of SILC as the stress progresses. Interestingly, this does not manifest itself in the I-V characteristics, where for the constant-voltage stress we see only an immediate degradation of subthreshold characteristics that remains roughly constant until breakdown. This suggests instead the generation of interface traps coupled with electron trapping in the oxide or the AlGaN barrier. In a gate voltage step-stress experiment, we see evidence of SILC at high gate voltages and a critical

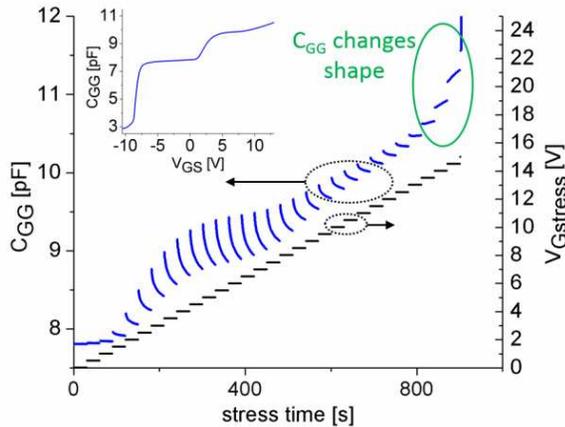


Fig. 8. Gate capacitance evolution at 500 kHz vs. stress time during a V_G step-stress experiment. C_{GG} is measured at $V_{Gstress}$ which is increasing by 0.5 V every 30 s. At $V_{Gstress} \sim 13.5$ V, the shape of C_{GG} changes. Inset is of 500 kHz C-V characteristics on an identical device up to 13 V.

gate voltage beyond which S degrades suddenly.

Many of these features are mirrored in our initial exploration of the C-V characteristics. In the future, we will continue to use I-V measurements and also leverage the unique abilities of C-V measurements, such as frequency dependence, to learn more about the physics of TDDB in GaN MIS-HEMTs.

CONCLUSIONS

In summary, we are developing new techniques to study TDDB in high-voltage GaN MIS-HEMTs. Our approach allows us to isolate the different roles of V_T shift, oxide trap formation and trapping, interface state generation, SILC and eventual breakdown.

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ACRONYMS

- MIS-HEMT: Metal-Insulator-Semiconductor-High Electron Mobility Transistor
 TDDB: Time-Dependent Dielectric Breakdown
 SILC: Stress-Induced Leakage Current
 FET: Field-Effect Transistor
 MOSFET: Metal-Oxide-Semiconductor Field Effect Transistor
 HPSMU: High Power Source Measurement Unit
 CMU: Capacitance Measurement Unit